

**DESCRIPTION:**

PMI MODEL NUMBER PTRAN-100M18G-SFB-3UVPX-10HP-MAH IS A TRANSCEIVER COVERING THE FREQUENCY RANGE OF 100 MHz TO 18 GHz. THE TRANSCEIVER FITS INTO A 3U OPEN VPX FORM FACTOR UTILIZING THE HIGH SPEED VITA 67 RF CONNECTOR. THIS UNIT UP-CONVERTS A 100 MHz TO 4 GHz TRANSMIT SIGNAL TO THE 2 TO 18 GHz RANGE. IT ALSO DOWN-CONVERTS A 100 MHz TO 18 GHz RECEIVED SIGNAL TO THE 100 MHz TO 4 GHz INTERMEDIATE FREQUENCY RANGE FOR ANALOG TO DIGITAL CONVERSION. A RECEIVE FILTER BANK INCORPORATES A 2-WAY ABSORPTIVE SWITCH TO SELECT AN INPUT, ALONG WITH TWO 6-WAY SWITCHES ALLOWING ONE OF SIX FILTER PATHS TO BE CHOSEN. A FILTER BANK IS USED ALSO ON THE TRANSMIT PATH, WITH TWO 6-WAY SWITCHES ALLOWING ONE OF SIX FILTER PATHS TO BE CHOSEN. THE UNIT IS MADE TO ATTACH TO AN FPGA CONTROLLER CARD ALLOWING FOR A TOTAL SOLUTION IN A 10 HP (2") FORM FACTOR.

**SPECIFICATIONS:**

• **INPUTS:** ..... **J1, J4A, J4B, J9, J10**

• **J1 INPUT:** ..... RF RECEIVE INPUT  
 FREQUENCY: ..... 100 MHz TO 18 GHz  
 POWER LEVEL: ..... -80 dBm TO -10 dBm TYPICAL  
 CONNECTOR: ..... SMPM (M)

• **J4A INPUT:** ..... IF1 INPUT  
 FREQUENCY: ..... 100 MHz TO 4 GHz  
 POWER LEVEL: ..... 0 dBm TYPICAL  
 CONNECTOR: ..... VITA 67

• **J4B INPUT:** ..... IF2 INPUT  
 FREQUENCY: ..... 100 MHz TO 4 GHz  
 POWER LEVEL: ..... 0 dBm TYPICAL  
 CONNECTOR: ..... VITA 67

• **J9 INPUT:** ..... LO1 INPUT  
 FREQUENCY: ..... 4 GHz TO 20 GHz  
 POWER LEVEL: ..... +10 dBm TYPICAL  
 CONNECTOR: ..... VITA 67

• **J10 INPUT:** ..... LO2 INPUT  
 FREQUENCY: ..... 4 GHz TO 20 GHz  
 POWER LEVEL: ..... +10 dBm TYPICAL  
 CONNECTOR: ..... VITA 67

• **OUTPUTS:** ..... **J3A, J3B, J6, J8, J11, J12**

• **J3A OUTPUT:** ..... IF1 OUTPUT  
 FREQUENCY: ..... 100 MHz TO 4 GHz  
 POWER LEVEL: ..... 0 dBm TYPICAL FOR LIMITED SDLVA CHANNEL  
 CONNECTOR: ..... VITA 67

• **J3B OUTPUT:** ..... IF2 OUTPUT  
 FREQUENCY: ..... 100 MHz TO 4 GHz  
 POWER LEVEL: ..... 0 dBm TYPICAL FOR LIMITED SDLVA CHANNEL  
 CONNECTOR: ..... VITA 67

• **J6 OUTPUT:** ..... RF TRANSMIT OUTPUT  
 FREQUENCY: ..... 100 MHz TO 18 GHz  
 POWER LEVEL: ..... 0 dBm TO +10 dBm TYPICAL  
 CONNECTOR: ..... SMPM (M)

• **J8 OUTPUT:** ..... RF TRANSMIT SAMPLE  
 FREQUENCY: ..... 100 MHz TO 18 GHz  
 POWER LEVEL: ..... -40 dBm TO -30 dBm TYPICAL  
 CONNECTOR: ..... SMPM (M)

• **J11 OUTPUT:** ..... LOG PROPORTIONAL DETECTED VIDEO OUTPUT (V1)  
 CONNECTOR: ..... SMA (F) (CABLED TO UMC (F))

• **J12 OUTPUT:** ..... THRESHOLD DETECTED VIDEO OUTPUT (V0)  
 CONNECTOR: ..... MEZZANINE CONNECTOR

• **POWER SUPPLY:** ..... PROVIDED BY OPEN VPX BACKPLANE THROUGH P0 CONNECTOR RATED FOR THE BELOW VOLTAGES  
 +12V: ..... 2 A  
 +5V: ..... 1.5 A  
 +3.3V: ..... 0.5 A  
 -12V: ..... 1 A

• **SIZE:** ..... 6.299" x 3.937" x 1.915"  
 (3U OPEN VPX CARD TO TAKE UP 10 HP WITH FPGA CARD)

• **RF CONNECTORS:** ..... VITA 67, 8 POSITION

• **DIGITAL CONTROL:** ..... TTL THROUGH MEZZANINE CONNECTOR ('0': 0 - 0.8 VOLTS), ('1' 2 - 5 VOLTS)

• **FINISH:** ..... GOLD PLATED

**NOTE: THE ABOVE SPECIFICATIONS ARE SUBJECT TO CHANGE OR REVISION**

- CONTROL LOGIC: ..... TTL ('0': 0 - 0.8 VOLTS), ('1' 2 - 5 VOLTS)
- TTL 1: ..... TRANSMIT PATH OUTPUT SELECT, RECEIVE FILTER BANK INPUT SELECT
  - 0 ..... OUTPUT TO TX FILTER BANK, RX-BACKPLANE/INPUT (J1)
  - 1 ..... OUTPUT TO RX FILTER BANK, RX - TRANSCEIVER INPUT
- TTL 2: ..... RECEIVE FILTER SELECT
  - 000 ..... THRU CHANNEL
  - 001 ..... CHANNEL 1
  - 010 ..... CHANNEL 2
  - 011 ..... CHANNEL 3
  - 100 ..... CHANNEL 4
  - 101 ..... CHANNEL 5
  - 110 ..... NOT DEFINED
  - 111 ..... NOT DEFINED
- TTL 3: ..... LINEAR OR LIMITED SDLVA RF OUTPUT CHANNEL
  - 0 ..... LIMITED RF OUTPUT CHANNEL
  - 1 ..... LINEAR RF OUTPUT CHANNEL
- TTL 4: ..... RECEIVE THRU CHANNEL OR DOWN-CONVERTED CHANNEL
  - 0 ..... THRU CHANNEL
  - 1 ..... DOWN-CONVERTED CHANNEL
- TTL 5: ..... IF1 OR IF2 OUTPUT SELECT
  - 0 ..... IF1 OUTPUT CHANNEL
  - 1 ..... IF2 OUTPUT CHANNEL
- TTL 6: ..... IF1 OR IF2 INPUT SELECT
  - 0 ..... IF1 INPUT CHANNEL
  - 1 ..... IF2 INPUT CHANNEL
- TTL 7: ..... TRANSMIT THRU CHANNEL OR UP-CONVERTED CHANNEL
  - 0 ..... THRU CHANNEL
  - 1 ..... UP-CONVERTED CHANNEL
- TTL 8: ..... TRANSMIT FILTER SELECT
  - 000 ..... THRU CHANNEL
  - 001 ..... CHANNEL 1
  - 010 ..... CHANNEL 2
  - 011 ..... CHANNEL 3
  - 100 ..... CHANNEL 4
  - 101 ..... CHANNEL 5
  - 110 ..... NOT DEFINED
  - 111 ..... NOT DEFINED
- TTL 9: ..... 5 BIT ATTENUATION CONTROL (1 dB STEPS)
  - 00000 ..... 0 dB ATTENUATION
  - 11111 ..... 31 dB ATTENUATION
- TTL 10: ..... LO SELECT
  - 00 ..... M1-LO1 M2-LO1
  - 01 ..... M1-LO1 M2-LO2
  - 10 ..... M1-LO2 M2-LO1
  - 11 ..... M1-LO2 M2-LO2
- TTL 11: ..... SDLVA THRESHOLD ADJUST
  - 000000 ..... LOWEST THRESHOLD LEVEL
  - 111111 ..... HIGHEST THRESHOLD LEVEL
- TTL 12: ..... SDLVA CTL A (ENABLE)
  - 0 ..... INTERNAL COMPARATOR TRIGGERED SPST
  - 1 ..... EXTERNAL TRIGGER ENABLE (SW CTL B)
- TTL 13: ..... SDLVA CTL B (TRIGGER)
  - 0 ..... LIMITED RF CH SPST SWITCH ON (INSERTION LOSS)
  - 1 ..... LIMITED RF CH SPST SWITCH OFF (ISOLATION)

**RECEIVE SWITCHED FILTER BANK:**

- J1 PATH GAIN: ..... 18 dB TYPICAL
- J7 PATH INSERTION LOSS: ..... 10 dB TYPICAL
- ISOLATION: ..... J1, J7 100 dB

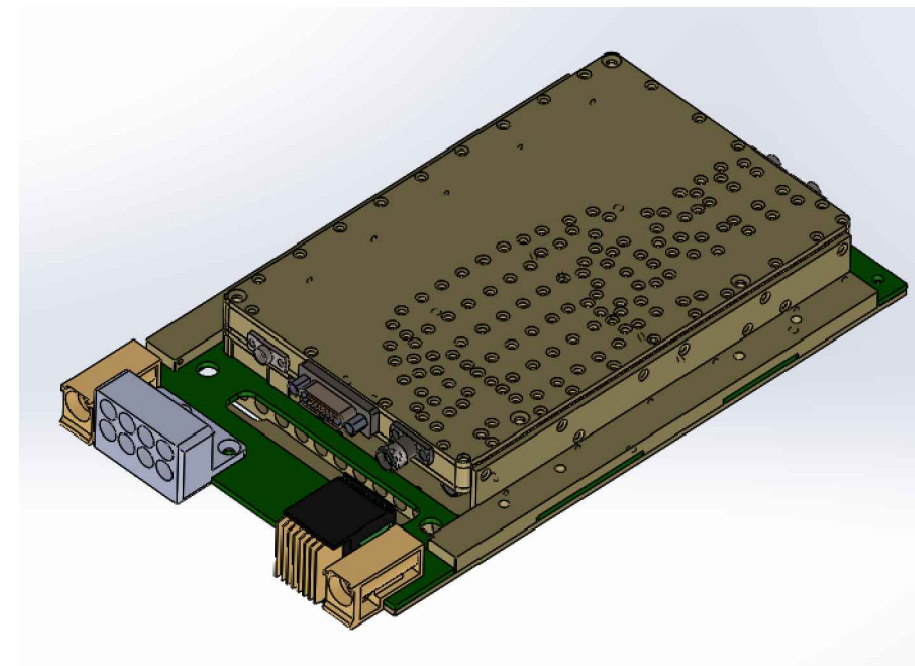
**TRANSMIT SWITCHED FILTER BANK:**

- GAIN: ..... 32 dB TYPICAL

**RECEIVE AND TRANSMIT SWITCHED FILTER BANKS:**

- VSWR OVER 90% PASSBAND: ..... 2 : 1 MAX
- SWITCHING SPEED: ..... 100 ns TYPICAL
- THRU CHANNEL PASSBAND: ..... 100 MHz TO 18 GHz
- CHANNEL 1 CENTER FREQUENCY: ..... 3400 MHz  
 3 dB BANDWIDTH: ..... 2000 MHz  
 REJECTION: ..... -40 dBc TYP 100 MHz - 2 GHz, -30 dBc MIN  
 ..... -40 dBc TYP 4.8 GHz - 18 GHz, -30 dBc MIN
- CHANNEL 2 CENTER FREQUENCY: ..... 5400 MHz  
 3 dB BANDWIDTH: ..... 2000 MHz  
 REJECTION: ..... -40 dBc TYP 100 MHz - 4 GHz, -30 dBc MIN  
 ..... -40 dBc TYP 6.8 GHz - 18 GHz, -30 dBc MIN
- CHANNEL 3 CENTER FREQUENCY: ..... 7400 MHz  
 3 dB BANDWIDTH: ..... 2000 MHz  
 REJECTION: ..... -40 dBc TYP 100 MHz - 6 GHz, -30 dBc MIN  
 ..... -40 dBc TYP 8.8 GHz - 18 GHz, -30 dBc MIN
- CHANNEL 4 CENTER FREQUENCY: ..... 9400 MHz  
 3 dB BANDWIDTH: ..... 2000 MHz  
 REJECTION: ..... -40 dBc TYP 100 MHz - 8 GHz, -30 dBc MIN  
 ..... -40 dBc TYP 10.8 GHz - 18 GHz, -30 dBc MIN
- CHANNEL 5 CENTER FREQUENCY: ..... 11400 MHz  
 3 dB BANDWIDTH: ..... 2000 MHz  
 REJECTION: ..... -40 dBc TYP 100 MHz - 10 GHz, -30 dBc MIN  
 ..... -40 dBc TYP 12.8 GHz - 18 GHz, -30 dBc MIN

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A1	ORIGINAL RELEASE	2/2/15	
	B1	ECN # 15-0126	10/22/15	



**SDLVA:**

- V0 (VIDEO COMPARATOR SIGNAL AMPLITUDE): ..... LVTTL
- VIDEO COMPARATOR DELAY: ..... 50 ns TYP.
- VIDEO COMPARATOR THRESHOLD LEVEL: ..... ADJUSTABLE WITH ANALOG VOLTAGE  
 ..... -60 dBm ±3.0 dB MAX.
- V1 (LOG VIDEO SIGNAL AMPLITUDE): ..... 1 VOLT MAX.
- LOG SLOPE: ..... 10 mV/dB INTO A 50-OHM LOAD (±1 mV) MAX.
- LOG RANGE: ..... -65 TO +5 dBm MIN.
- LOG LINEARITY: ..... ±1.75 dB (-40°C TO +85°C) MAX.
- PULSE RANGE: ..... 100 ns TO 250 us
- RISE TIME: ..... 35 ns MAX.
- SETTling TIME TO ±1dB: ..... 50 ns TYP.
- RECOVERY TIME: ..... 350 ns MAX.
- CW IMMUNITY RANGE: ..... TSS TO -45 dBm (1 dB DEGRADATION)
- PULSE CONSIDERED "CW": ..... 1 ms TYP.
- REJECTION TIME: ..... 1 ms TYP.
- DROOP: ..... 1 dB MAX.
- SPST ISOLATION: ..... 70 dB TYP.
- SPST SWITCH SPEED: ..... 20 ns TYP.
- SW CTL A (ENABLE): ..... TTL 0: INTERNAL COMPARATOR TRIGGERED SPST  
 ..... TTL 1: EXTERNAL TRIGGER ENABLE (SW CTL B)
- SW CTL B (TRIGGER): ..... TTL 0: LIMITED RF CH SPST SWITCH ON (INSERTION LOSS)  
 ..... TTL 1: LIMITED RF CH SPST SWITCH OFF (ISOLATION)

**PMI CONFIDENTIAL AND PROPRIETARY**

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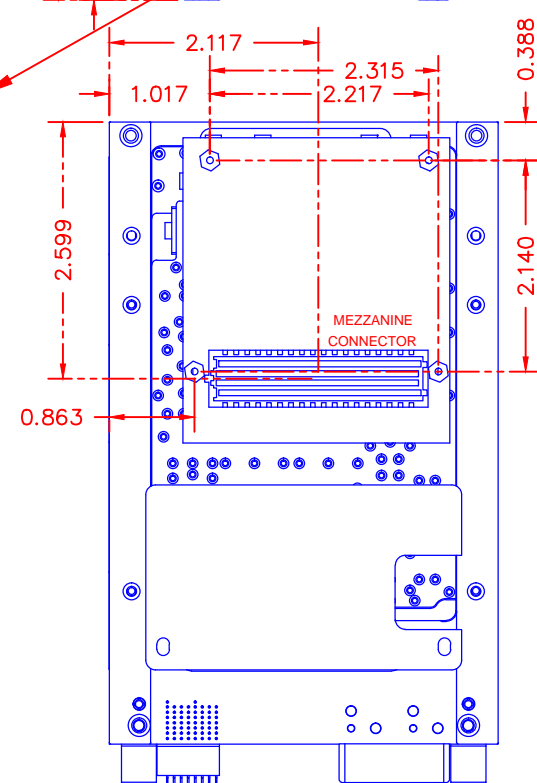
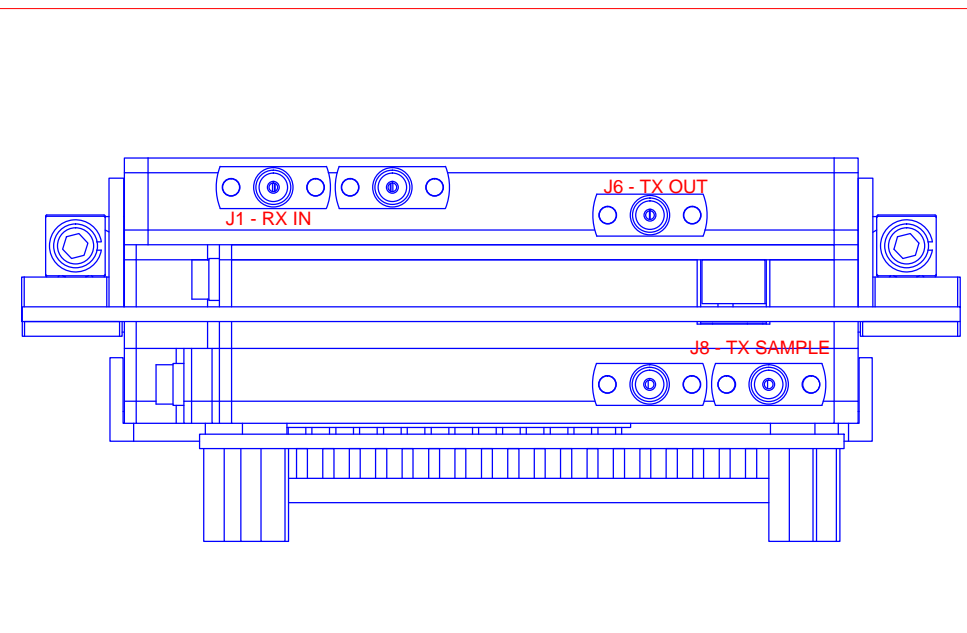
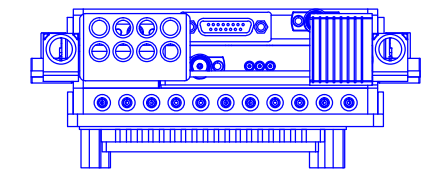
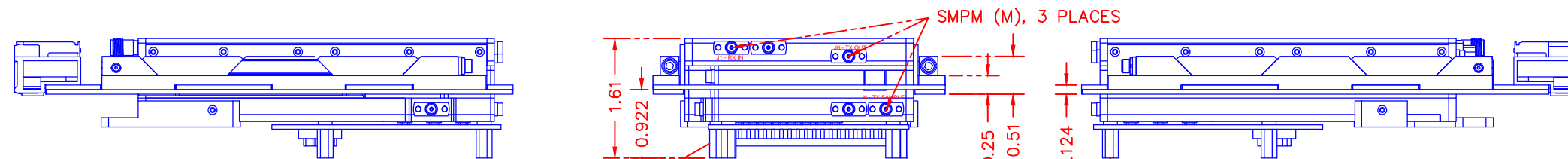
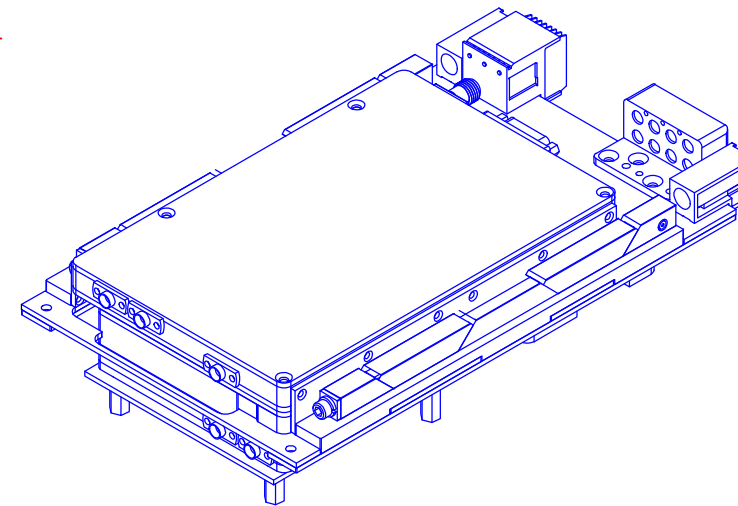
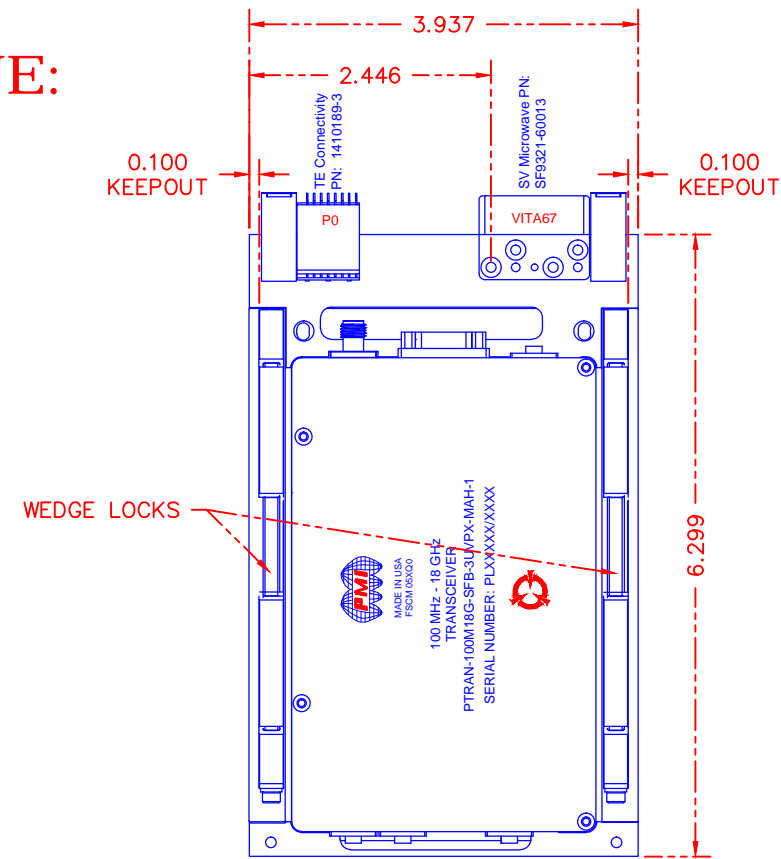


APPROVALS		DATE	TITLE		
DRAWN	<i>DPD</i>	2/2/15	PRODUCT FEATURE		
CHECKED			PTRAN-100M18G-SFB-3UVPX-10HP-MAH		
ISSUED			SIZE	FSCM NO.	DWG NO.
			B	05XQ0	27024281
			SCALE	N:S	SHEET 1 OF 5
					REV. B1

ALL DIMENSIONS ARE IN INCHES  
 TOLERANCES:  
 X.XX ±0.020  
 X.XXX ±0.010

# MECHANICAL OUTLINE:

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A1	ORIGINAL RELEASE	2/2/15	
	B1	ECN # 15-0126	10/22/15	



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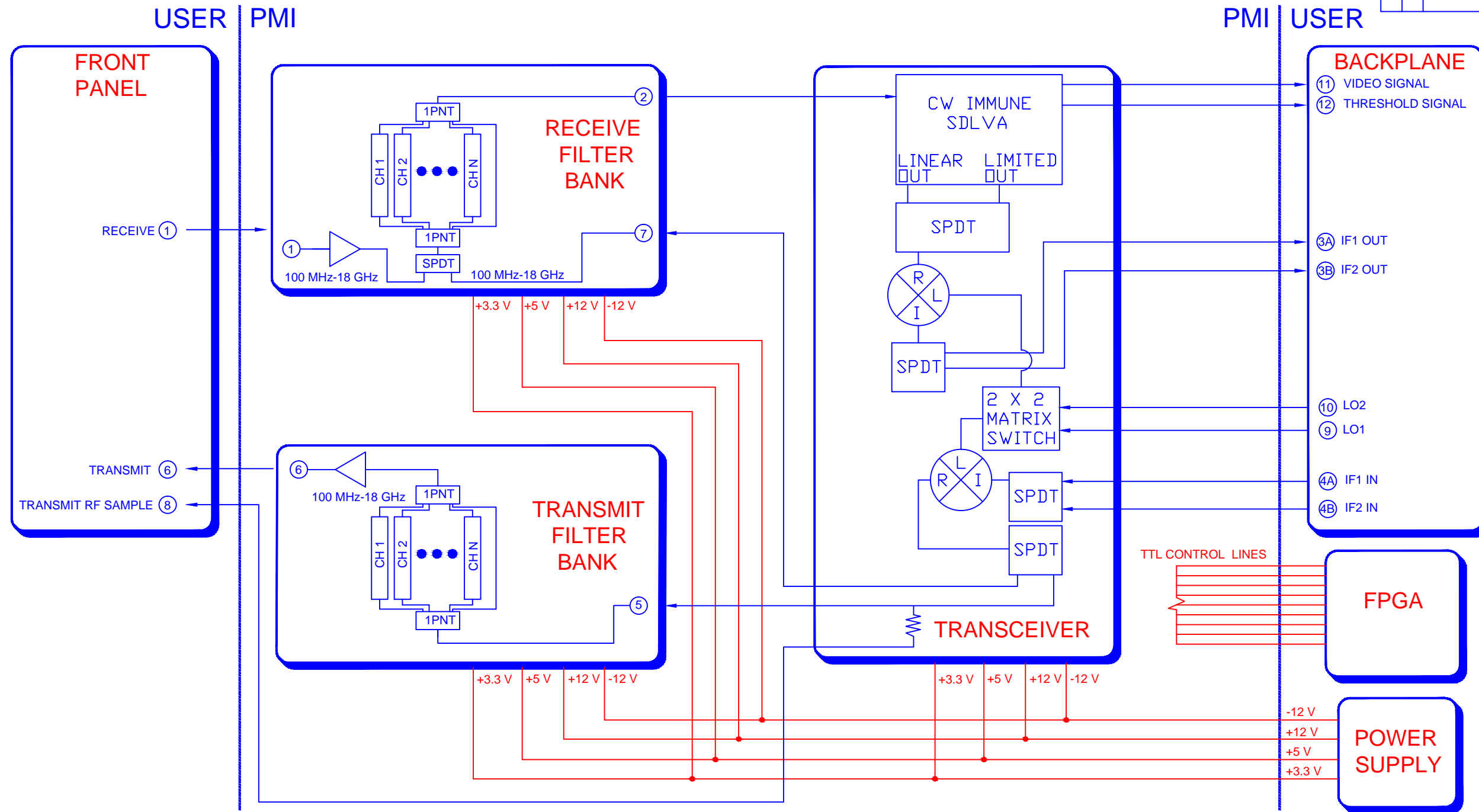
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ISSUED			SIZE B	REV. B1
			FSCM NO. 05XQ0	DWG NO. 27024281
			SCALE N:S	SHEET 2 OF 5

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
A1		ORIGINAL RELEASE	2/2/15	
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# BLOCK DIAGRAM:



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			B	05XQ0	27024281
			SCALE	N:S	SHEET 3 OF 5
					REV. B1

# INTERCONNECT TABLE:

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A1	ORIGINAL RELEASE	2/2/15	
	B1	ECN # 15-0126	10/22/15	

FMC PIN	CN 2				FMC PIN
-	GND	1	2	GND	-
H5	N/C	3	4	N/C	H4
H8	TTL1	5	6	TTL2A (LSB)	H7
H11	TTL2B	7	8	TTL2C (MSB)	H10
H14	TTL3	9	10	TTL4	H13
H17	TTL5	11	12	TTL6	H16
H20	TTL7	13	14	TTL8A (LSB)	H19
H23	TTL8B	15	16	TTL8C (MSB)	H22
H26	TTL9A (LSB)	17	18	TTL9B	H25
H29	TTL9C	19	20	TTL9D	H28
H32	TTL9E (MSB)	21	22	TTL 10A (LSB)	H31
H35	TTL10B (MSB)	23	24	N/C	H34
H38	N/C	25	26	N/C	H37
-	GND	27	28	GND	-
-	N/C	29	30	N/C	-

FMC PIN	CN 3				FMC PIN
-	GND	1	2	GND	-
G3	N/C	3	4	N/C	G2
G7	TTL11A (LSB)	5	6	TTL11B	G6
G10	TTL11C	7	8	TTL11D	G9
G13	TTL11E	9	10	TTL11F (MSB)	G12
G16	TTL12	11	12	TTL13	G15
G19	SDLVA V0	13	14	N/C	G18
G22	N/C	15	16	N/C	G21
G25	N/C	17	18	N/C	G24
G28	N/C	19	20	N/C	G27
G31	N/C	21	22	N/C	G30
G34	N/C	23	24	N/C	G33
G37	N/C	25	26	N/C	G36
-	GND	27	28	GND	-
-	N/C	29	30	N/C	-

FMC PIN	CN 4				FMC PIN
-	GND	1	2	GND	-
D9	N/C	3	4	N/C	D8
D12	N/C	5	6	N/C	D11
C11	N/C	7	8	N/C	C10
D15	N/C	9	10	N/C	D14
C15	N/C	11	12	N/C	C14
D18	N/C	13	14	N/C	D17
C19	N/C	15	16	N/C	C18
D21	N/C	17	18	N/C	D20
C23	N/C	19	20	N/C	C22
D24	N/C	21	22	N/C	D23
D27	N/C	23	24	N/C	D26
C27	N/C	25	26	N/C	C26
-	GND	27	28	GND	-
-	N/C	29	30	N/C	-

P0 Pin	Function
a1	Vs2 (+3.3 V)
a2	Vs2 (+3.3 V)
a3	Vs3 (+5 V)
a4	NC (NVMRO)
a5	NC (SM1)
a6	NC (GA0)
a7	NC (TRST)
a8	GND (GND)

P0 Pin	Function
b1	Vs2 (+3.3 V)
b2	Vs2 (+3.3 V)
b3	Vs3 (+5 V)
b4	NC (SYSRESET)
b5	NC (SM0)
b6	NC (GA1)
b7	NC (TMS)
b8	NC (RES_BUS+)

P0 Pin	Function
c1	Vs2 (+3.3 V)
c2	Vs2 (+3.3 V)
c3	Vs3 (+5 V)
c4	GND (GND)
c5	GND (GND)
c6	GND (GND)
c7	GND (GND)
c8	NC (RES_BUS-)

P0 Pin	Function
d1	NC (No Pad)
d2	NC (No Pad)
d3	NC (No Pad)
d4	-12V (-12V Aux)
d5	NC (3.3V_AUX)
d6	NC (+12V_AUX)
d7	NC (TDI)
d8	GND (GND)

P0 Pin	Function
e1	Vs1 (+12 V)
e2	Vs1 (+12 V)
e3	Vs3 (+5 V)
e4	GND (GND)
e5	GND (GND)
e6	GND (GND)
e7	NC (TDO)
e8	NC (REF_CLK+)

P0 Pin	Function
f1	Vs1 (+12 V)
f2	Vs1 (+12 V)
f3	Vs3 (+5 V)
f4	NC (SM3)
f5	NC (GA4)
f6	NC (GA2)
f7	GND (GND)
f8	NC (REF_CLK-)

P0 Pin	Function
g1	Vs1 (+12 V)
g2	Vs1 (+12 V)
g3	Vs3 (+5 V)
g4	NC (SM2)
g5	NC (GAP)
g6	NC (GA3)
g7	NC (TCK)
g8	GND (GND)

VITA 67 Pin	Function
A1	J4A (IF1 IN)
A2	J4B (IF2 IN)
A3	J9 (LO1)
A4	J10 (LO2)
B1	NC
B2	NC
B3	J3A (IF1 OUT)
B4	J3B (IF2 OUT)

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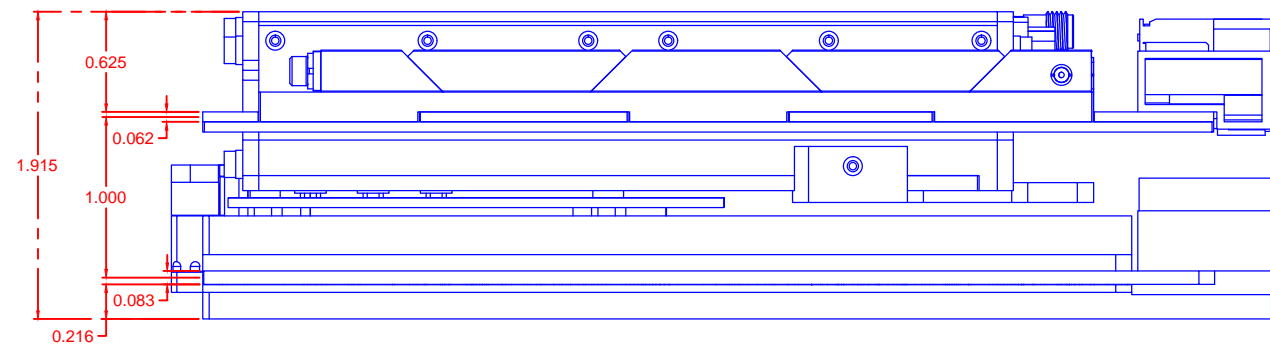
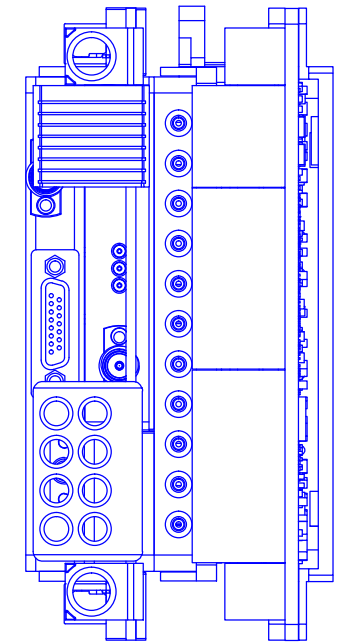
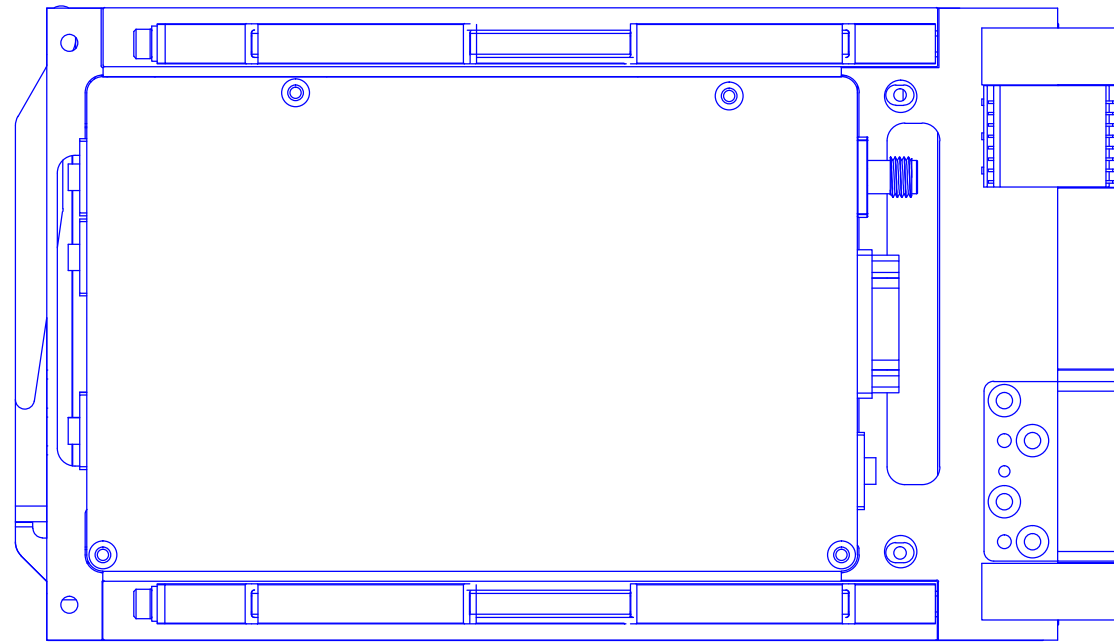
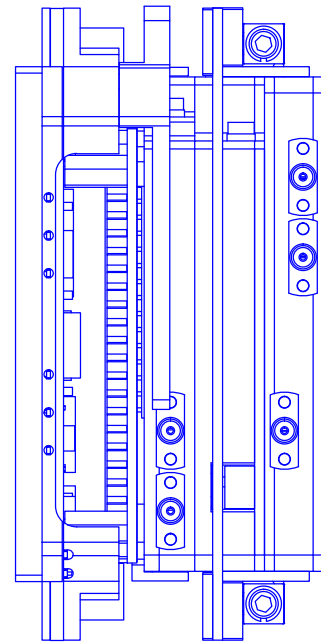
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			B	05XQ0	27024281
			SCALE	N:S	SHEET 4 OF 5

REV. B1

# FULLY ASSEMBLED WITH FPGA CARD (FPGA CARD NOT INCLUDED)

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	B1	ECN # 15-0126	10/22/15	



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					REV. B1